



IFSYS-5043 Bluetooth Module
Product Datasheet

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1 GENERAL DESCRIPTION

The IFSYS-5043 Bluetooth® Module is a complete Class 2 *Bluetooth* module incorporating an antenna, on-board oscillators, a UART or USB interface for communication to a host processor, and an internal codec. IFSYS-5043 is based on the Cambridge Silicon Radio (CSR) BC03 Multimedia External single chip *Bluetooth* solution.

Based on a small form factor design, IFSYS-5043 is intended for easy integration into OEM/ODM designs. IFSYS-5043 supports different software configurations, which enable the module to work in standalone mode for embedded applications, or in hosted mode interfaced to a host processor.

1.1 Key Features

- Supports built-in *Bluetooth* Profiles for stand-alone applications
- Bluetooth® V2.0 compliant and FCC (modular) certified
- High speed UART interface supports communication at up to 921kbps
- Small form factor surface mounted package facilitates integration into space constrained embedded devices and equipment
- Low power requirements of Bluetooth technology make the IFSYS-5043 module suited to integration into battery-powered equipment.
- Single voltage supply.
- Built in DSP supports computationally intensive operations.
- Choice between using the built-in codec or an external codec.

1.2 Usage Modes

The IFSYS-5043 is suitable for deployment in the following types of designs:

- In a hosted design in which the module operates with an HCI interface, driven by a host processor or controller
- Standalone design in which the application, profiles and Bluetooth stack code all reside within the module.

1.3 Summary Specifications

Hardware features

- Complete HCI compliant module featuring single chip CSR BC03 Multimedia External *Bluetooth* device
- 53-pin surface mount package
- Built-in antenna
- Class 2 Bluetooth module

Physical interfaces

- UART interface (4 signals) - TXD, RXD, RTS# and CTS#.
- PCM/Codec interface (4 signals) – PCM-SYNC, PCM-CLK, PCM-IN, PCM-OUT.
- GPIO interface (12 signals) – PIO [0..11]
- Analog IO interface (3 signals) – AIO0, AIO1, AIO3
- SPI interface for firmware download – MOSI, MISO, CLK, CSB
- Differential Stereo Audio Input
- Differential Stereo Audio Output

Electrical specifications

- Temperature: Operational: 0°C to +70°C, Storage: -20°C to +85°C
- Transmitter power: *Bluetooth* Class 2 device (4dBm max)
- Bluetooth* transmitting range: Up to 10m (free-air)
- Power supply & voltage levels:
 - Supply VDD: 3.3Vdc +/- 0.3V
 - Differential Stereo Audio Input/Output: 0 – 1.8Vdc voltage range per differential signal
 - GPIO interface: 0 – 1.8Vdc
 - UART interface: 0 – 3.3Vdc

Applications [Note: Dependent on Bluetooth profiles]

- Wireless Speakers with Remote Control (A2DP-Sink and AVRCP)
- Car Handsfree designs with Echo-Cancellation (HFP and HSP)
- High Performance Telephony Headsets

Certification/Compliance

- Bluetooth* V2.0 Specification compliant (QD ID: B012734)
- FCC certified (FCC ID: VBR5043)
- RoHS compliant design - IFSYS-5043 meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

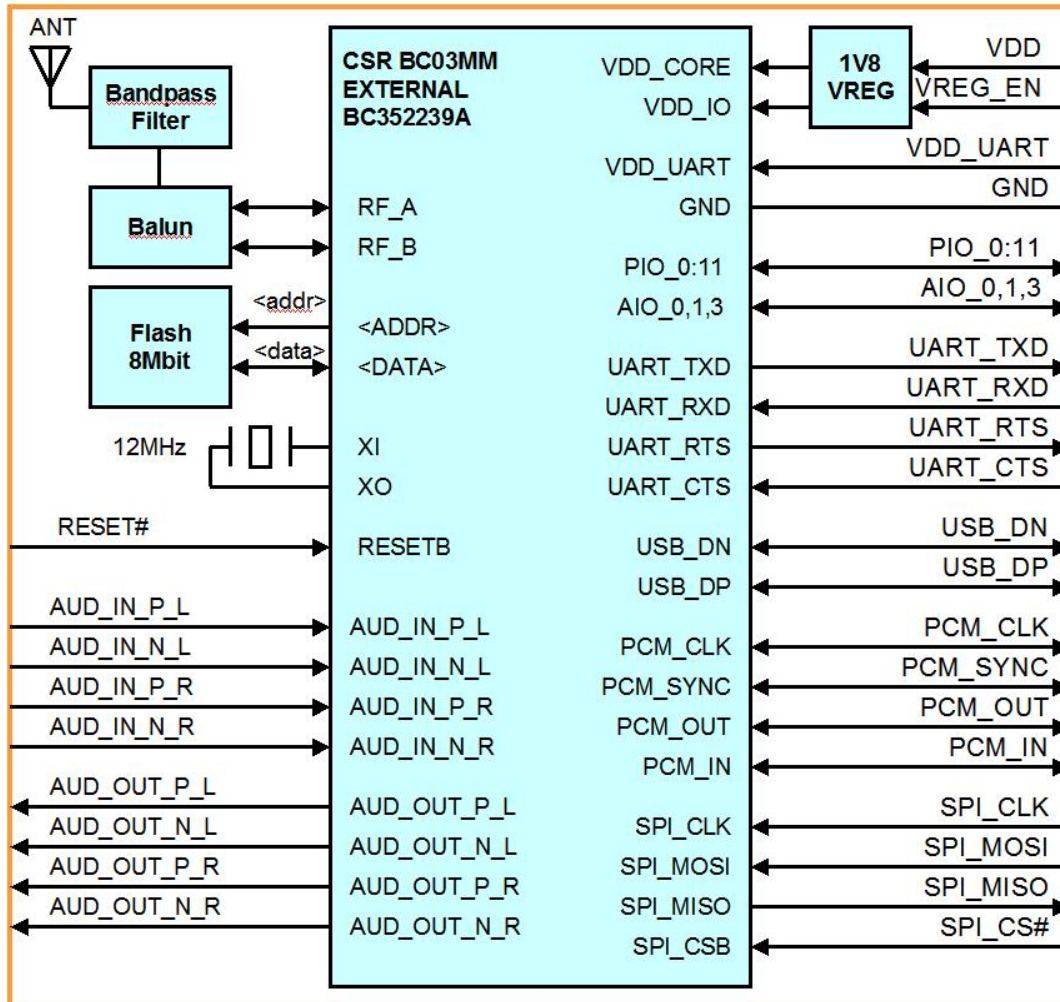
Dimensions

- 16mm (L) x 36.5mm (W) x 2.2mm (H)
- Weight: approx. 2g

2 PRODUCT DESCRIPTION

2.1 Block Diagram

This section provides the product specifications.



2.3 Device Pinout & Description

Pin Number	Name	I/O	Reset State	Supply Domain	Type	Description
1,7,12, 21, 30, 35, 39, 42, 50, 51, 53	GND					Ground
2	PIO0	I/O	I Pull-down	1.8V	Bi-directional	Programmable input/output line
3	AUDIO_OUT_N_LEFT	O		1.8V	Analog	Audio output negative (left side)
4	AUDIO_OUT_P_LEFT	O		1.8V	Analog	Audio output positive (left side)
5	AUDIO_OUT_N_RIGHT	O		1.8V	Analog	Audio output negative (right side)
6	AUDIO_OUT_P_RIGHT	O		1.8V	Analog	Audio output positive (right side)
8	AUDIO_IN_P_RIGHT	I		1.8V	Analog	Audio input positive (right side)
9	AUDIO_IN_N_RIGHT	I		1.8V	Analog	Audio input negative (right side)
10	AUDIO_IN_P_LEFT	I		1.8V	Analog	Audio input positive (left side)
11	AUDIO_IN_N_LEFT	I		1.8V	Analog	Audio input negative (left side)
13	AIO0	I/O	O low	1.8V	Bi-directional 1.8V	Programmable analog/digital input/output line
14	AIO1	I/O	O low	1.8V	Bi-directional 1.8V	Programmable analog/digital input/output line
15	AIO3	I/O	O low	1.8V	Bi-directional 1.8V	Programmable analog/digital input/output line
16	VDD_USB			VDD_USB	+3.3V Supply	Supply for USB/UART Block
17	USB_DP	I/O	I pull-down	VDD_USB	Bi-directional	USB Data Plus
18	USB_DN	I/O	I pull-down	VDD_USB	Bi-directional	USB Data Minus
19	VDD			VDD	+3.3V Supply	Power
20	UART_CTS	I	I pull-down	VDD_USB	CMOS input	UART clear to send active low
22	UART_RX	I	I pull-down	VDD_USB	CMOS input	UART data input
23	UART_RTS	O	O pull-up	VDD_USB	CMOS output, tri-state	UART request-to-send active low
24	UART_TX	O	O pull-up	VDD_USB	CMOS output, tri-state	UART data output
25	VREG_EN	I		VDD		Module enable pin, active high
26	PIO6	I/O	I weak pull-down	1.8V	Bidirectional with programmable strength internal pull-up/down	
27	PIO7	I/O	I weak pull-down	1.8V	Bidirectional with programmable strength internal pull-up/down	
28	PIO4	I/O	I weak pull-down	1.8V	Bidirectional with programmable strength internal pull-up/down	
29	PIO5	I/O	I weak pull-down	1.8V	Bidirectional with programmable strength internal pull-up/down	
31	SPI_CS#	I	I weak pull-up	1.8V	CMOS input with weak internal pull-up	
32	SPI_CLK	I	I weak pull-down	1.8V	CMOS input with weak internal pull-down	

Pin Number	Name	I/O	Reset State	Supply Domain	Type	Description
33	SPI_MISO	O	O tri-stated weak pull-down	1.8V	CMOS output, tri-state, with weak internal pull-down	
34	SPI_MOSI	I	I weak pull-down	1.8V	CMOS input with weak internal pull-down	
36	PCM_IN	I	I weak pull-down	1.8V	CMOS input, with weak internal pull-down	
37	PCM_SYNC	I/O	I weak pull-down	1.8V	Bi-directional with weak internal pull-down	
38	PCM_CLK	I/O	I weak pull-down	1.8V	Bi-directional with weak internal pull-down	
40	PCM_OUT	O	O tri-stated weak pull-down	1.8V	Output, tri-state, with weak internal pull-down	
41	RESET#	I	I weak pull-up	1.8V	CMOS input with weak internal pull-up	Reset if low. Input debounced must be low for >5ms to cause a reset
43	PIO3	I/O	I weak pull-down	1.8V	Bidirectional with programmable strength internal pull-up/down	
44	PIO2	I/O	I weak pull-down	1.8V	Bidirectional with programmable strength internal pull-up/down	
45	PIO11	I/O	I weak pull-down	1.8V	Bidirectional with programmable strength internal pull-up/down	
46	PIO10	I/O	I weak pull-down	1.8V	Bidirectional with programmable strength internal pull-up/down	
47	PIO9	I/O	I weak pull-down	1.8V	Bidirectional with programmable strength internal pull-up/down	
48	PIO8	I/O	I weak pull-down	1.8V	Bidirectional with programmable strength internal pull-up/down	
49	PIO1	I/O	I weak pull-down	1.8V	Bidirectional with programmable strength internal pull-up/down	
52	EXT_ANT				External antenna	

3 ELECTRICAL CHARACTERISTICS

3.1 Absolute Maximum Ratings

Rating	Minimum	Maximum	Unit
Storage Temperature	-40	+150	°C
Supply Voltage: VDD, VDD_USB	-0.4	3.7	V
Other Terminals	-0.4	VDD+0.4	V

3.2 Recommended Operating Conditions

Operating Condition	Minimum	Maximum	Unit
Operating Temperature Range	0	+70	°C
Supply Voltage			
VDD	2.7	3.7	V
VDD_USB	3.1	3.3	V

3.3 Digital Terminal

Digital Terminals	Minimum	Typical	Maximum	Unit
Input Voltage Levels				
V _{IL} input logic level low	-0.4	-	+0.4	V
V _{IH} input logic level high	1.26	-	2.2	V
Output Voltage Levels				
V _{OL} output logic level low (I _O = 4.0mA)	-	-	0.4	V
V _{OH} output logic level high (I _O = 4.0mA)	1.4	-	-	V
Input and Tri-state Current with				
Strong pull-up	-100	-40	-10	μA
Strong pull-down	+10	+40	+100	μA
Weak pull-up	-0.5	-1.0	-0.2	μA
Weak pull-down	+0.2	+1.0	+0.5	μA
I/O pad leakage current	-1.0	0.0	+1.0	μA
C _I Input Capacitance	1.0	9	5.0	pF

3.4 USB Terminal

USB Terminals	Minimum	Typical	Maximum	Unit
VDD_USB for correct USB operation	3.1		3.6	V
Input threshold				
V _{IL} input logic level low	-	-	0.3 VDD_USB	V
V _{IH} input logic level high	0.7 VDD_USB	-	-	V
Input leakage current	-1	1	5	μA
C _I Input capacitance	2.5		10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V _{OL} output logic level low	0	0	0.2	V
V _{OH} output logic level high	2.8	-	VDD_USB	V

Note:

(1) Internal USB pull-up disabled.

3.5 Auxiliary ADC

Auxiliary ADC	Minimum	Typical	Maximum	Unit	
Resolution	-	-	8	Bits	
Input voltage range (LSB size = VDD_ANA/255)	0	-	1.8	V	
Accuracy (Guaranteed monotonic)	INL	-1	-	1	LSB
	DNL	0	-	1	LSB
Offset	-1	-	1	LSB	
Gain Error	-0.8	-	0.8	%	
Input Bandwidth	-	100	-	kHz	
Conversion time	-	2.5	-	μ S	
Sample rate(1)	-	-	700	samples/S	

3.6 Auxiliary DAC

Auxiliary DAC	Minimum	Typical	Maximum	Unit
Resolution	-	-	8	
Average output step size ⁽¹⁾	12.5	14.5	17.0	mV
Output Voltage		monotonic(1)		
Voltage Range	0	-	1.8	V
Current range	-10.0	-	+0.1	mA
Minimum output voltage (I _o =100mA)	0.0	-	0.2	V
Maximum output voltage (I _o =10mA)	1.5	-	1.8	V
High Impedance leakage current	-1	-	+1	μ A
Offset	-220	-	+120	mV
Integral non-linearity ⁽¹⁾	-2	-	+2	LSB
Settling time (50pF load)	-	-	10	μ S

3.7 Stereo Codec

3.7.1 Input Stage/Microphone Amplifier

Input Stage/Microphone Amplifier	Minimum	Typical	Maximum	Unit
Input full scale at maximum gain	-	4	-	mVrms
Input full scale at minimum gain	-	400	-	mVrms
Gain resolution	-	3	-	dB
Distortion at 1kHz	-	-	-74	dB
Input referenced rms noise in 15kHz bandwidth	-	8	-	Vrms
3dB Bandwidth	-	17	-	kHz
Input impedance	-	20	-	k Ω
THD+N (microphone input) @ 30mV rms input	-	-66	-	dB

3.7.2 Output stage/Loudspeaker driver

Output Stage/Loudspeaker Driver	Minimum	Typical	Maximum	Unit
Output power into 32	-	30	-	mWpk
Output voltage full scale swing	-	2.0	-	Vpk-pk
Output current drive (at full scale swing)(1)	10	20	40	mA
Output full scale current (at reduced swing)(1)	-	75	-	mA
Distortion and noise (relative to full scale), THD	-	-75	-	dBc
Allowed Load: resistive	16	-	O.C	Ω
Allowed Load: capacitive	-	-	500	pF

3.8 Power Consumption

Typical Average Current Consumption		
VDD=1.8V Temperature = +20°C Output Power = +4dBm		
Mode	Average	Unit
SCO connection HV3 (30ms interval Sniff Mode) (Slave)	21	mA
SCO connection HV3 (30ms interval Sniff Mode) (Master)	21	mA
SCO connection HV3 (No Sniff Mode) (Slave)	28	mA
SCO connection HV1 (Slave)	42	mA
SCO connection HV1 (Master)	42	mA
ACL data transfer 115.2kbps UART no traffic (Master)	5	mA
ACL data transfer 115.2kbps UART no traffic (Slave)	22	mA
ACL data transfer 720kbps UART (Master or Slave)	45	mA
ACL data transfer 720kbps USB (Master or Slave)	45	mA
ACL connection, Sniff Mode 40ms interval, 38.4kbps UART	3.2	mA
ACL connection, Sniff Mode 1.28s interval, 38.4kbps UART	0.45	mA
Parked Slave, 1.28s beacon interval, 38.4kbps UART	0.55	mA
Standby Mode (Connected to host, no RF activity)	47	µA
Reset (RESETB low)	15	µA
DSP		
DSP core (including PM memory access)		
Minimum (NOP)	0.25	mA/MIPS
Maximum (MAC)	0.65	mA/MIPS
DSP memory access (DM1 or DM2)	0.15	mA/MIPS
CODEC		
Microphone inputs and ADC / channel	0.85	mA
DAC and loudspeaker driver, no signal / channel ⁽¹⁾	1.4	mA
Digital audio processing subsystem	8	mA

Note: (1) Power consumption increase is >5% for maximum signal.

4 DESIGN GUIDELINES

4.1 Power Supply

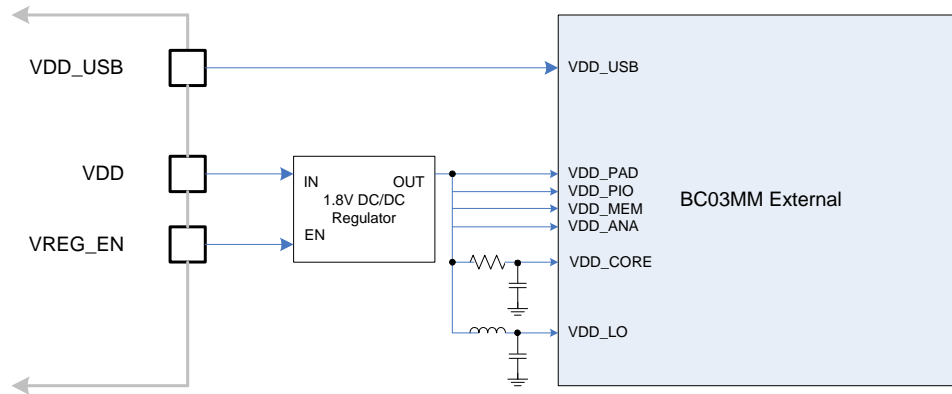


Figure 4.1:

An on-board 1.8V DC/DC Converter is used to power the PIO ports, Flash RAM, Analog block, and digital circuitry. VDD_USB is supplied directly from an external source, or it can be connected together with VDD. Please observe VDD_USB voltage limit for proper USB functionality.

VREG_EN provides flexibility of turning ON/OFF the module in a battery-operated application such as stereo headset, with the expense of additional components.

Place a bypassing capacitor between VDD and GND as near as possible to VDD pin.

5 INTERFACING GUIDELINES

5.1 Interfacing with External Codec

The interface for the digital audio bus shares the same pins as the PCM Interface. This means that each of the audio busses are mutually exclusive in their usage. The pin out for the PCM interface with alternative pin descriptions are listed in Table 5.1.

PCM Interface	SPDIF Interface	I2S Interface
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC		WS
PCM_CLK		SCK

Table 5.1: Alternative pin descriptions of PCM Interface

5.2 I2S Interface

The digital audio interface supports the industry standard formats for I2S (left-justified), left-justified (LJ) or right-justified(RJ)⁽¹⁾. The interface shares the same pins as the PCM interface as shown in Table 5.1 and the timing diagram is shown in Figure 5.1.

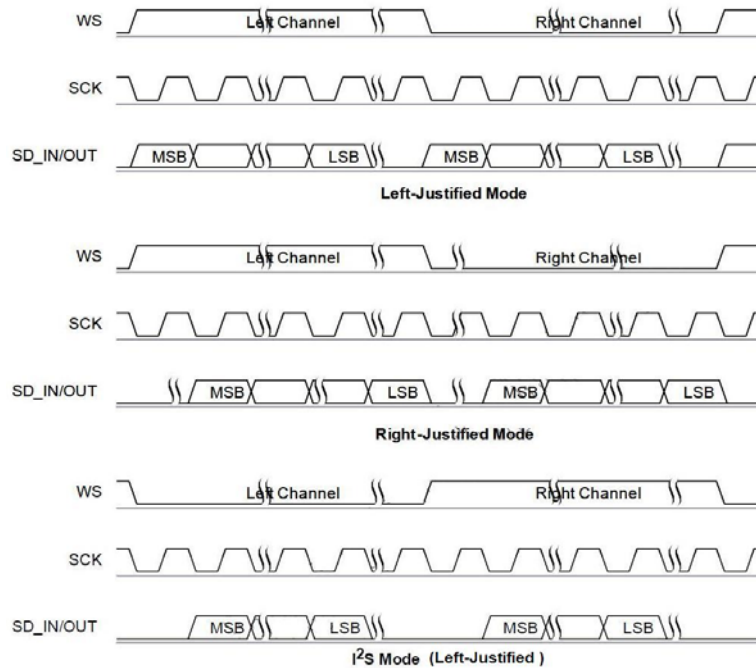


Figure 5.1: Digital Audio Interface Modes

The internal representation of audio samples within BlueCore3-Multimedia External is 16-bit and data on SD_OUT is limited to 16-bit per channel. On SD_IN, if more than 16-bit per channel is present will round considering the 17th bit.

SCK typically operates 64 x WS frequency and cannot be less than 36 x WS.

Parameter	Minimum	Typical	Maximum	Unit
SCK Frequency	-	-	6.2	MHz
WS Frequency	-	-	96	kHz

Table 5.2: Digital Audio Interface Slave Timing

Parameter	Minimum	Typical	Maximum	Unit
SCK Frequency	-	-	6.2	MHz
WS Frequency	-	-	96	kHz

Table 5.3: Digital Audio Interface Master Timing

5.3 Reference codec interfacing

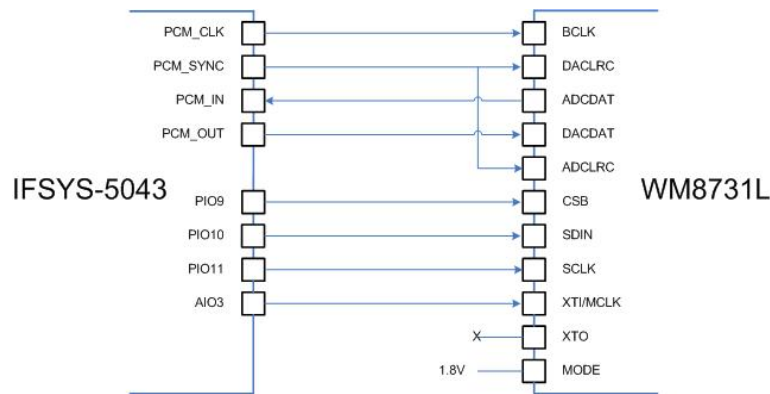


Figure 5.2: Interfacing IFSYS-5043 with WM8731L

The diagram above shows an example of interfacing IFSYS-5043 to a Wolfson WM8731L codec. The arrow indicates signal direction.

- WM8731L master clock

WM8731L master clock is provided by IFSYS-5043 AIO3 output, which is configured to output clock signal same as crystal frequency, 12MHz.

- I2S audio signal

IFSYS-5043 is the I2S master providing the bit clock signal (BCLK), word clock signal (DACLRC), and the audio data. (DACDAT). ADCLRC and ADCDAT are only relevant if WM8731L audio input is used (as Line In or Mic input). If PCM_IN is not used, it is recommended to connect it to ground.

- WM8731L MCU control signal

The WM8731L control interface is configured to 3-wire interface (SPI) by setting MODE input to HIGH. The functions of these lines are to program/configure WM8731L registers. IFSYS5043 control the data lines via software controlled GPIOs.

6 DIMENSIONS

6.1 Module Dimensions

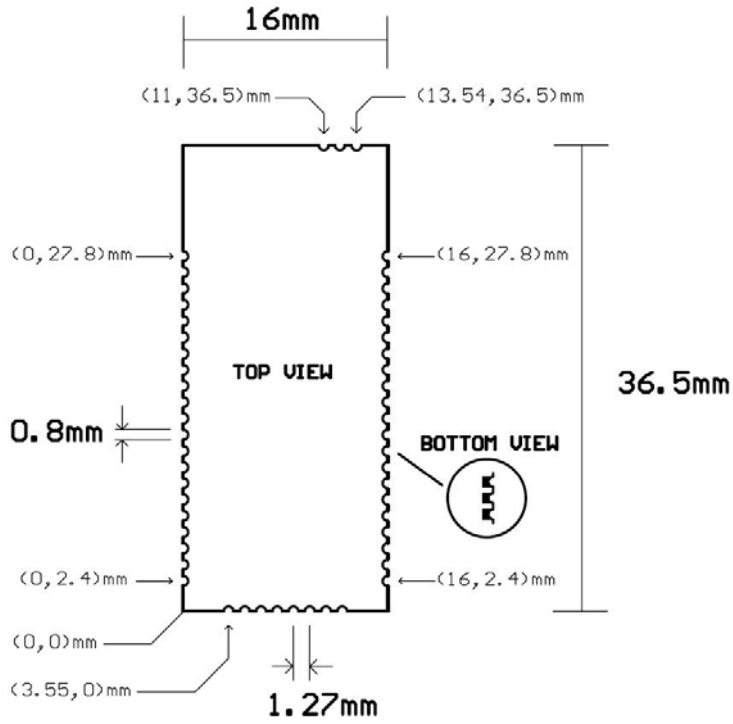


Figure 6.1: Module Dimension

6.2 Recommendations for PCB layout

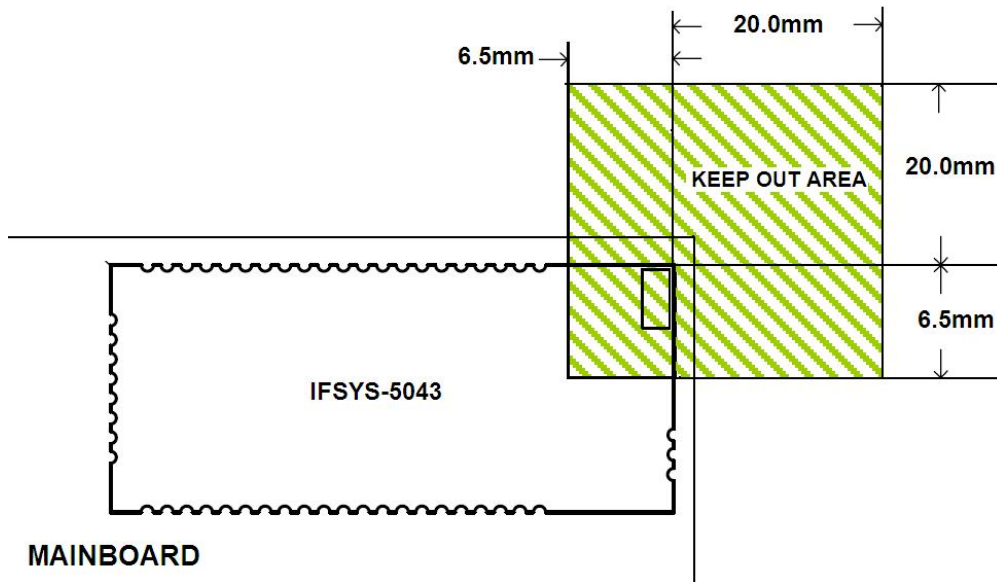


Figure 6.2: Recommended PCB layout

Figure 6.2 illustrates recommended PCB design around the antenna of IFSYS-5043 when the module is placed at the edge of a PCB.

- Any metalisation around the keep out area will degrade the antenna performance. Therefore, do not place copper on all layer under the keep out area, and avoid using metal case around the module.
- On the top layer of the mainboard, ensure that there are no exposed copper under the module as the modules has vias and test points on its bottom layer.

7 SOLDERING GUIDELINES

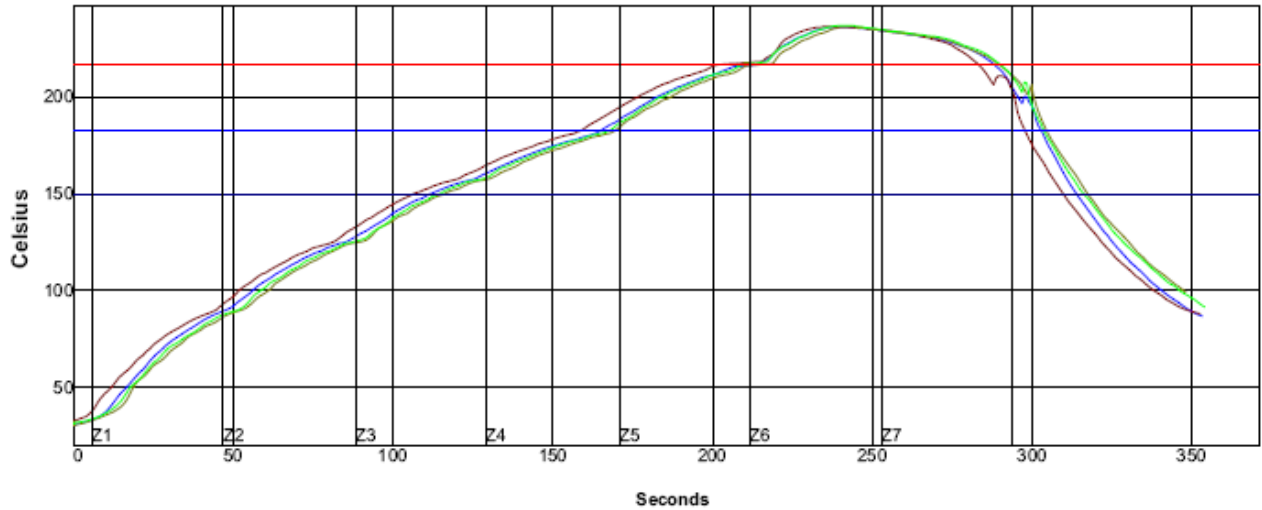
7.1 Soldering Profile

IFSYS-5043
Recommended Soldering Profile

Process: LEADFREE

Setpoints (Celsius)							
Zone	1	2	3	4	5	6	7
Top	110	140	170	190	228	252	225
Bottom	110	140	170	190	228	252	225

Conveyor Speed (inch/min): 22.0



PWI= 61%	Max Rising Slope	Preheat 150-183C	Soak Time 183-217C	Reflow Time /217C	Peak Temp					
TC1	1.8	60%	53.4	-46%	49.1	22%	73.6	35%	236.4	28%
TC2	1.7	57%	53.8	-45%	47.6	2%	71.9	28%	236.6	31%
TC3	1.8	59%	52.9	-48%	45.8	-23%	77.9	52%	236.4	29%
TC4	1.7	57%	53.5	-46%	42.9	-61%	78.8	55%	236.9	38%
Delta	0.1		0.9		6.2		6.8		0.5	

Process Window:

Solder Paste:				
Statistic Name	Low Limit	High Limit	Units	
Max Rising Slope (Target=0.0) (Calculate Slope over 20 Seconds)	0.0	3.0	Degrees/Second	
Preheat Time 150-183C	40	90	Seconds	
Soak Time 183-217C	40	55	Seconds	
Time Above Reflow - 217C	40	90	Seconds	
Peak Temperature	230	240	Degrees Celsius	

8 BLUETOOTH QUALIFICATIONS, REGULATORY AND ENVIRONMENTAL SPECIFICATIONS

For reference, this section represents the regulatory qualifications for this product. It is also possible for specific customer requirements to be added to the list of certification requirements for custom designs. Please contact iFoundry for assistance with those requirements.

8.1 Regulatory Specifications

Test Type	Test Standard	Description	Notes
FCC	FCC Part 15B&C:2006	Conducted Emissions Radiated Emissions Carrier Frequency Separation Spectrum Bandwidth Number of Hopping Frequencies Average Frequency Dwell Maximum Peak Power RF Conducted Spurious Emissions Band Edge Compliance (Conducted & Radiated) Peak Power Spectral Density Maximum Permissible Exposure	
ETSI	EN 300 328 V1.6.1: 2004	Equivalent Isotropic Radiated Power Maximum Spectral Power Density Frequency Range Transmitter Spurious Emissions (Conducted) Receiver Spurious Emissions (Conducted & Radiated)	

8.2 Environmental Specifications

Please note that these are target specifications.

8.2.1 Temperature and Humidity

Detail	Min.	Max.	Notes
Operating temperature	0°C	+70°C	(32°F – 158°F)
Storage temperature	-22°C	+85°C	(-4°F – 185°F)
Operating Relative Humidity	90%	-	Relative humidity at 40°C (104°F)
Condensation Immunity	Operational after 5 minutes in chamber set at 40°C and 95% RH		

8.2.2 Shock and Vibration Testing

Detail	Pass Criteria
Product drop test - 1 metre drop onto 6mm plywood surface supported by concrete surface.	All six sides and two opposing corners without enclosure or functional failure
Shipping package drop test - 2 meter drop onto 6mm concrete surface.	All six sides and two opposing corners without Product enclosure or Product functional failure, or detectable cosmetic damage

9 STATUS INFORMATION

The status of this Data Sheet is **Production Information**.

IFS Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values. All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-Production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values. All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications. Production Data Sheets supersede all previous document versions.

10 SUPPORT & CONTACT INFORMATION

Technical support knowledge base, and updated drivers can be obtained from iFoundry Systems website at www.ifoundrysys.com.